

ent B1
a third insulated material disposed over said tunnel oxide layer, said select gate and
said floating gate; and C

a control gate formed on said third insulated material.

SUB C2 7 15 12. A structure of an Electrically Erasable Programmable Read-Only Memory
(EEPROM), comprising:

a silicon substrate having a source/drain region;

a tunnel oxide layer disposed over said silicone substrate;

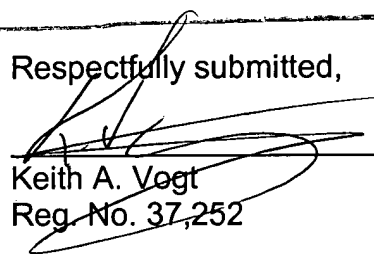
Rule 126 B2
a select gate disposed over said tunnel oxide layer, wherein said select gate is defined
by a conductive layer covered with a first insulated material thereon and comprises a sidewall made
of a second insulated material; C

a floating gate aligned to one side of said select gate;

a third insulated material disposed over said tunnel oxide layer, said select gate and
said floating gate; and

a control gate formed on said third insulated material, said control gate partially
covers said third insulating material.

Respectfully submitted,


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